WHAT IS CLAIMED IS:

1. A system for processing digital signals, comprising:

a pointer follower to receive a first digital signal having a first signal frame, a first embedded payload and a pointer follower ("PF") pointer, extract said first embedded payload from said first digital signal and forward said first embedded payload;

an elastic buffer in electrical connection with said pointer follower operable to receive, delay and forward said first embedded payload;

a pointer generator to receive said first embedded payload and a synchronization pulse and construct a new digital signal comprising said first embedded payload, a new signal frame, and a pointer generator ("PG") pointer, wherein the location of said new signal frame within said new digital signal is determined according to said synchronization pulse; and

a synchronization module to generate said synchronization pulse according to a predetermined schedule and communicate said synchronization pulse to said pointer generator.

2. The system of Claim 1, further comprising:

a first comparator operable to compare the value of said PF pointer and the value of said PG pointer and generate a pointer offset signal; and

a second comparator operable to compare said pointer offset signal to a target offset signal, generate an increment/decrement request signal based on the comparison, and communicate the increment/decrement request signal to said elastic buffer; and

wherein said elastic buffer delays said embedded payload according to said increment/decrement signal.

3. The system of Claim 2, further comprising:

a PG counter synchronized according to said synchronization pulse;

a PF counter to track the location of said signal frame of said first digital signal; and

a third comparator to measure the offset between said PG counter and said PF counter.

4. The system of Claim 3, wherein the value of said PG pointer is determined by the offset between said PG counter and said PF counter, the value of said PF pointer, and the delay imposed by said elastic buffer.

5. The system of Claim 1, wherein said first digital signal has a SONET signal format.

6. The system of Claim 1, wherein said first digital signal is a packet based signal.

7. A system for processing digital signals comprising:

a first adder circuit comprising:

a first pointer follower to receive a first digital signal having a first signal frame, a first embedded payload and a first pointer follower ("PF") pointer, extract said first embedded payload from said first digital signal and forward said first embedded payload;

a first elastic buffer in electrical connection with said first pointer follower operable to receive, delay and forward said first embedded payload;

a first pointer generator to receive said first embedded payload and a synchronization pulse and construct a first new digital signal comprising said first embedded payload, a first new signal frame and a first pointer generator ("PG") pointer, wherein the location of said first new signal frame in said first new digital signal is determined according to said synchronization pulse; and

a second adder circuit comprising:

a second pointer follower to receive a second digital signal having a second signal frame, a second embedded payload and a second pointer follower pointer ("PF pointer"), extract said second embedded payload from said second digital signal and forward said second embedded payload;

a second elastic buffer in electrical connection with said second pointer follower operable to receive, delay and forward said second embedded payload; and

a second pointer generator to receive said second embedded payload and construct a second new digital signal

comprising said second embedded payload, a second new signal frame and a second PG pointer, wherein the location of said second new signal frame within said second new digital signal is determined by said synchronization pulse and wherein said second new signal frame is aligned with said first new signal frame; and

a synchronization module to generate said synchronization pulse according to a predefined schedule and operable to communicate said synchronization pulse to said first adder circuit and to said second adder circuit.

8. The system of Claim 7, wherein said first digital signal and said second digital signal are a working copy and a protection copy, respectively, of the same digital signal.

9. The system of Claim 8, wherein said first digital signal and said second digital signal are in a packet based format.

10. The system of Claim 7, wherein:

said first adder circuit further comprises:

a first pointer comparator to compare the value of said first PG pointer to the value of said first PF pointer and generate a first pointer offset signal based on the comparison; and

a first offset comparator to compare said first pointer offset signal to a first target offset signal, generate a first increment/decrement request signal, and communicate said first increment/decrement signal to said first elastic buffer,

wherein said first elastic buffer is operable to delay said first embedded payload based on said first increment/decrement request signal; and

said second adder circuit further comprises:

a second pointer comparator to compare the value of said second PG pointer to the value of said second PF pointer and generate a second pointer offset signal based on the comparison; and

a second offset comparator to compare said second pointer offset signal to a second target offset signal, generate a second increment/decrement request signal, and communicate said second increment/decrement request signal to said second elastic buffer, wherein said second elastic buffer is operable to delay said second embedded payload based on said second increment/decrement signal; and

wherein said first elastic buffer and said second elastic buffer forward said first embedded payload and said second embedded payload, respectively, in payload alignment.

11. The system of Claim 10 wherein:

said first adder circuit further comprises:

a first pointer generator counter ("PG counter") synchronized according to said synchronization pulse;

a first pointer follower counter ("PF counter") to track the location of said first signal frame of said first digital signal; and

a first counter comparator to measure the offset between said PG counter and said PF counter; and

said second adder circuit further comprises:

a second PG counter synchronized according to said synchronization pulse; and

a second PF counter to track the location of said second signal frame of said second digital signal; and

a second counter comparator to measure the offset between said second PG counter and said second PF counter.

12. The system of Claim 11 wherein said first target offset signal and said second target offset signal represent equal target offsets.

13. The system of Claim 11, wherein:

the value of said first PG pointer is determined by the value of said first PF pointer, the offset between said first PG pointer counter and said first PF pointer counter and the delay imposed by said first elastic buffer; and

wherein the value of said second PG pointer is determined by the value of said second PF pointer, the offset between said second PG pointer counter and said second PF pointer counter and the delay imposed by said second elastic buffer

14. The system of Claim 10, wherein the value of said first PG pointer and the value of said second PG pointer are equal.

15. The system of Claim 10, wherein said first new digital signal and said second new digital signal are in frame alignment and payload alignment.

16. The system of Claim 10, wherein said first digital signal and said second digital signal are a working copy and a protection copy, respectively, of the same digital signal.

17. The system of Claim 10, wherein said first digital signal and said second digital signal are in a packet based format.

18. The system of Claim 10, further comprising:

a PF comparator operable to compare said first PF pointer to said second PF pointer and generate a PF difference signal; and

an adder operable to add the PF difference signal to a base target offset signal to derive said first target offset signal; and

wherein said first offset comparator is operable to compare said first offset signal to said first pointer offset signal to derive said first increment/decrement request signal.

19. A method for processing digital signals comprising:

receiving a first digital signal at a first pointer follower ("PF"), having a first signal frame, a first embedded payload and a first PF pointer;

extracting said first embedded payload from said first digital signal;

forwarding said first embedded payload;

delaying said first embedded payload at a first elastic buffer and forwarding said first embedded payload to first pointer generator;

constructing a first new digital signal comprising said first embedded payload, a first new signal frame and a first pointer generator ("PG") pointer at said first pointer generator, wherein the location of said first new signal frame within said first new digital signal is determined according to a synchronization pulse; and

receiving a second digital signal at a second pointer follower having a second signal frame, a second embedded payload and a second PF pointer, extracting said second embedded payload from said second digital signal;

forwarding said second embedded payload;

delaying said second embedded payload at a second elastic buffer and forwarding said second embedded payload to a second pointer generator; and

constructing a second new digital signal comprising said second embedded payload, a second new signal frame and a second PG pointer at said second pointer generator, wherein the location of said second new signal frame is determined according to said synchronization pulse; and

generating said synchronization pulse according to a predefined schedule and communicating said synchronization pulse to said first pointer generator and said second pointer generator.

20. The method of Claim 19, wherein said first digital signal and said second digital signal are a working copy and a protection copy, respectively, of the same digital signal.

21. The method of Claim 20, wherein said first digital signal and said second digital signal are in a packet based format.

22. The method of Claim 19, further comprising:

comparing the value of said first PG pointer to the value of said first PF pointer at a first pointer comparator and generating a first pointer offset signal based on the comparison;

comparing said first pointer offset signal to a first target offset signal at a first offset comparator;

generating a first increment/decrement request signal at said first offset comparator based on the comparison between said first pointer offset signal and said first target offset signal;

communicating said increment/decrement request signal to said first elastic buffer, wherein said first elastic buffer is operable to delay said first embedded payload based on said first increment/decrement request signal; and

comparing the value of said second PG pointer to the value of said second PF pointer at a second pointer comparator and generating a second pointer offset signal based on the comparison; and

comparing said second pointer offset signal to a second target offset signal at a second offset comparator, generating a second increment/decrement request signal, and communicating said increment/decrement request signal to said second elastic buffer, wherein said second elastic buffer is operable to delay said second embedded payload based on said second increment/decrement request signal; and

forwarding said first embedded payload and said second embedded payload in payload alignment.

23. The method of Claim 22 further comprising

determining a first counter offset between a first PG counter and a first PF counter at a first counter comparator; and

determining a second counter offset between a second PG counter and a second PF counter at a second counter comparator.

24. The method of Claim 23 wherein said first target offset and said second target offset represent equal target offsets.

25. The method of Claim 23, wherein:

the value of said first PG pointer is determined by the value of said first PF pointer, the offset between said first PG

pointer counter and said first PF pointer counter and the delay imposed by said first elastic buffer; and

wherein the value of said second PG pointer is determined by the value of said second PF pointer, the offset between said second PG pointer counter and said second PF pointer counter and the delay imposed by said second elastic buffer

26. The method of Claim 22, wherein the value of said first PG pointer and the value of said second PG pointer are equal.

27. The method of Claim 22, wherein said first new digital signal and second new digital signal are in frame alignment and payload alignment.

28. The method of Claim 22, wherein said first digital signal and said second digital signal are a working copy and a protection copy, respectively, of an original digital signal.

29. The method of Claim 22, wherein said first digital signal and said second digital signal are in a packet based format.

30. The method of Claim 22, further comprising:

comparing said first PF pointer to said second PF pointer, generating a PF difference signal;

adding said PF difference signal to a base target offset signal to form said first target offset signal; and

comparing said first target offset signal to said first pointer offset signal to derive said first increment/decrement request signal.

31. The method of Claim 22, further comprising:

communicating said first new digital signal and said second new digital signal to a switch; and

hitlessly switching between said first new digital signal and said second new digital signal.

32. A system for processing a digital signal, comprising:

a pointer follower to receive a first digital signal having a first signal frame, a first embedded payload and a pointer follower ("PF") pointer, extract said first embedded payload from said first digital signal and forward said first embedded payload;

an elastic buffer in electrical connection with said pointer follower operable to receive, delay and forward said first embedded payload;

a pointer generator to receive said first embedded payload and a synchronization pulse and construct a new digital signal comprising said first embedded payload, a new signal frame, and a pointer generator ("PG") pointer, wherein the location of said new signal frame within said new digital signal is determined according to said synchronization pulse;

a synchronization module to generate said synchronization pulse according to a predetermined schedule and communicate said synchronization pulse to said pointer generator;

a first comparator operable to compare the value of said PF pointer and the value of said PG pointer and generate a pointer offset signal; and

a second comparator operable to compare said pointer offset signal to a target offset signal, generate an increment/decrement request signal based on the comparison, and communicate the increment/decrement request signal to said elastic buffer; and

wherein said elastic buffer delays said embedded payload according to said increment/decrement signal.